Principles and Applications of the ICL7660 CMOS Voltage Converter

INTRODUCTION

This application note describes a device originally designed to solve the specific problem of needing a negative supply when only a positive supply is available. This is very common, and occurs, for example, in systems using dynamic RAMs where the three-supply devices require a low current body bias supply of around −5V. Negative supply voltage is also desired in systems with a lot of digital logic (at +5V) but containing a small analog section using A/D converters, such as the ICL7107 or ICL7109 and/or op amps and comparators, operating on ground referenced signals. In all these cases, the current requirement and regulation are not very demanding, but nevertheless, generating such a −5-V supply is usually expensive and inefficient. Typically, a large number of discrete and integrated-circuit components are needed to convert the common +5-V line into a negative one, or to add an extra output to the main supply, the backplane wiring, etc.

This problem is solved by the ICL7660, a monolithic CMOS power supply circuit offering unique performance advantages over previously available devices. With the addition of only two non-critical capacitors (for charge pump and storage), it performs the complete supply voltage conversion from positive to negative for any input voltage between +1.5V and +10V, and provides the complementary output voltage of −1.5V to −10V. (An additional diode is needed for voltages above 6.5V.) The device operates by charging a pump capacitor to the input supply voltage and then applying the capacitor across the output supply, transferring the necessary charge to a open-circuit storage capacitor.

The ICL7660 delivers an open-circuit output equal to the negative of the input voltage to within 0.1%. Capable of providing 20 mA, the device has a power-conversion efficiency of about 98% for load currents of 2 to 5 mA. The use of two or more 7660s extends the device's capability, as will be shown later.

PRINCIPLES OF OPERATION

Since the 7660 multiplies either positive or negative voltages by a factor of two, it can be considered a simple voltage doubler. This basic voltage doubling operation is shown in Figure 1, where S1 and S3 are the switches used to charge C1, and S2 and S4 transfer the charge to C2. It differs from most voltage doublers in that the usual blocking diodes are replaced by on-chip active MOS transistor switches.

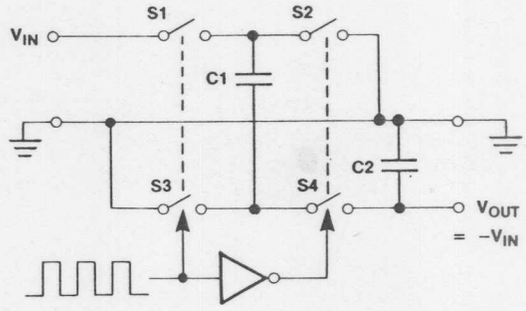

Figure 1. Idealized Voltage Doubler

For a negligible load, clearly the voltage inversion will be nearly perfect, with only a tiny charge being lost to stray capacitance. With a significant load, the behavior is more complex.

The amount of charge transferred from C1 to C2 depends upon the amount lost from C2 to the load, and this charge must be made up by C1 from the basic power supply. The switches themselves also have series resistance, leading to further theoretical complications, but the net result is a typical overall output impedance of around 55Ω (100Ω max), provided that the capacitors are sufficiently large. For the natural oscillation frequency of the built-in oscillator (approx. 10kHz) values of 10μF are adequate.

The complete implementation of this function is achieved on a single CMOS chip, as shown in Figure 2.

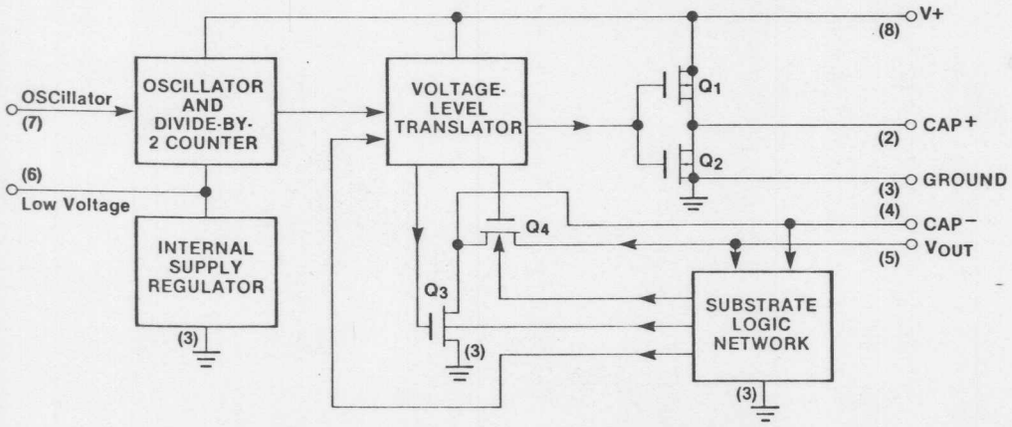

Figure 2. Block Diagram of complete chip

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The 7660 contains all the necessary conversion functions on-chip, except for the external pump and output reservoir capacitors and is made with a low-threshold CMOS technology using p- and n-channel transistors that turn on at 0.6 V. The low power dissipation, simplicity, and small chip size of CMOS make it a near-ideal technology for this application.

The 7660 contains an RC oscillator, a series voltage regulator, a voltage-level translator, and a logic network (Fig. 2). The logic network senses the voltage on the sources and drains of the two output n-channel transistors Q_3 and Q_4 and ensures that their substrates are always correctly biased.

POWER EFFICIENCY

In the case where a capacitor is charged and discharged between two voltages, V_1 and V_2, the energy lost is defined by

$$E = \frac{C\,(V_1^2 - V_2^2)}{2}$$

where C is value of the capacitor in farads and E is the lost energy. If $V_1 - V_2$ is very small compared with V_1, the percentage energy loss is also small, given as:

$$\frac{100\,(V_1^2 - V_2^2)}{2\,(V_1^2)}$$

At the limit, when $V_2 = V_1$, no energy is lost. If the values of C_1 and C_2 in Fig. 1 are made very large and their impedances at the switching frequency are very low compared with the load resistance, energy-conversion efficiencies approaching 100% can be obtained . Energy is lost only by a change of voltage during the transfer of charge into and out of a capacitor.

DETAILED DESCRIPTION

Oscillator—Divider—Regulator

The 7660's oscillator (Fig. 3) drives a conventional divide-by-2 counter whose principal function is to supply a 50% duty cycle output (at half the input frequency) to the voltage-level translator circuit. The conventional static counter requires a two-phase clock, and supplies an output signal and its complement.

When the output of inverter A_1 is switched high, capacitor C charges positively until inverter A_2 (which has a high input-voltage trip point) switches its output low, to turn on transistor Q_1. Q_1 in turn forces the ratioed-inverter latch A_4—A_5 to switch its output low. C then discharges negatively until inverter A_3 (which has a low input-voltage trip point) switches its output high, turning on transistor Q_2. The output of Q_2 resets A_4—A_5 and restarts the cycle.

Since the oscillator has a high input impedance of about 1MΩ, it may be driven from an external source such as a TTL gate or equivalent, or its frequency may be lowered by the addition of an external capacitor. At room temperature with a +5-V supply and no external capacitor, the oscillator frequency will be 10kHz. The internal capacitance is about 10pF..

A series voltage regulator consisting of zener reference diode Z_1, resistor R_1, and source-follower p-channel transistor Q_3 provides a partially regulated supply for all the low-voltage circuitry on the chip. The regulator can supply up to −5 V (with respect to the positive power supply) for input supply voltages of about 6 V and higher. Because of the modest size of Q_3, the voltage regulator not only reduces power consumption at high supply voltages, but also limits the maximum current taken by the oscillator and the divide-by-2 counter.

The LV terminal can be used to short out the on-chip series regulator for better operation at low supply voltages. With the Low-Voltage terminal connected to ground, operation with an input supply voltage as low as 1 V is possible. At higher voltages, however, it is mandatory that this terminal be open, in order to allow the internal voltage regulator to stop device latchup and avoid internal damage.

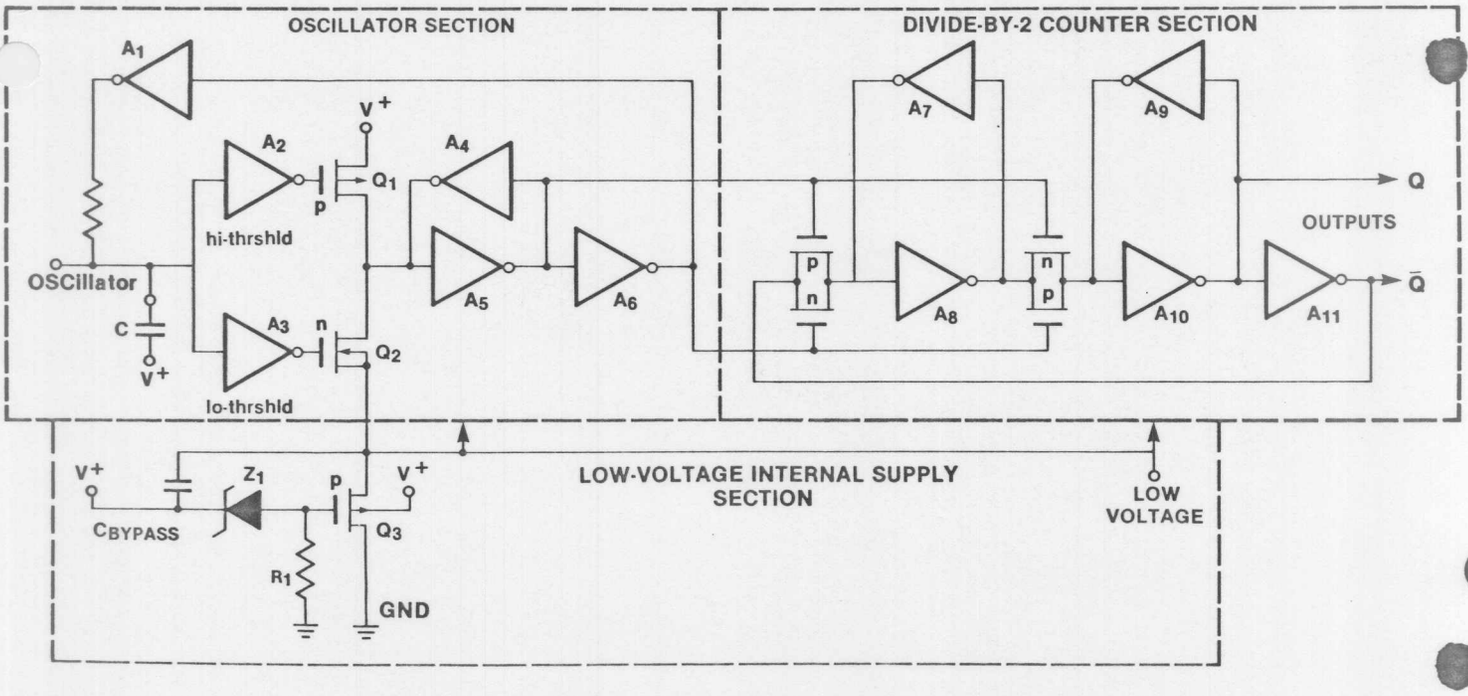
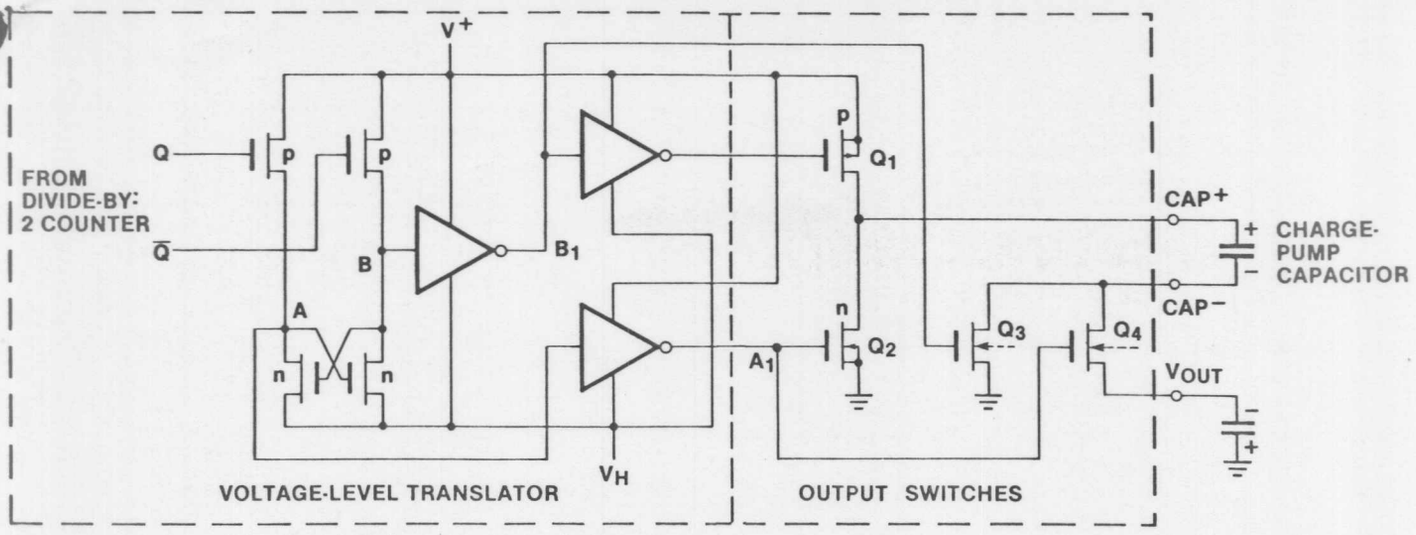


Figure 3. The 7660's oscillator, divider and internal regulator



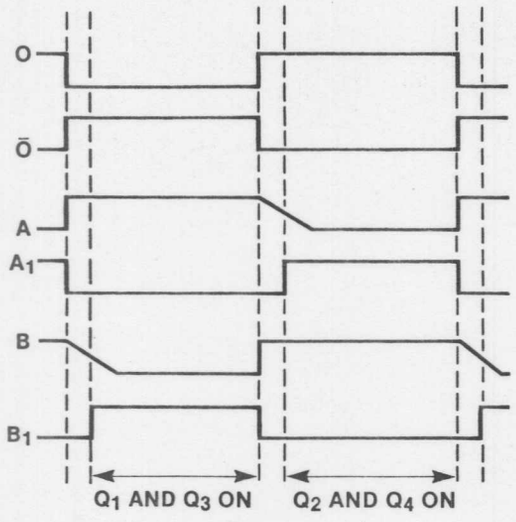


Figure 4. The 7660's output switches and voltage-level translator circuit

The Level-Translators and Output Switches

The level translators (Fig. 4) provide switching signals to the gates of the four output transistors, Q_1 through Q_4, with amplitudes equal to the sum of the output and supply voltages. They also ensure that a break-before-make sequence takes place as switching alternates between charge and pump configurations.

The Substrate Logic Network

The substrate logic network (Fig. 5) is the most critical part of the converter chip. Its two main functions are to make sure that the substrates of Q_2 and Q_4 (Fig. 4) are never forward-biased with respect to their sources and drains, and to establish the most negative voltage of any part of the circuit in either the charge or the pump cycles. This internal negative supply, V_H, is used to power the level translators. It drives the gate of either Q_3 or Q_4 to a voltage similar to that of the sources to ensure transistor turn off.

Transistors Q_3 and Q_4 require special drive considerations, since the sources and drains are inverted on each device during pump and charge phases. Consider Q_3's operation, for example. During the charge phase, the most positive source/drain terminal is connected to the external charge-pump capacitor. This terminal is then, by definition, the drain, whereas the source which is more negative is connected to ground. To minimize Q_3's resistance, it is also desirable to connect its substrate to ground and not to the output voltage or to V_H, since reverse-biasing the substrate of an MOS transistor with respect to its source increases its threshold voltage, and therefore the ON resistance.

During the pumping phase, the external capacitor's negative terminal is shifted negatively by a voltage approximately equal to the supply voltage. In this case, the most negative source/drain terminal is connected to the negative side of the external capacitor (and thus becomes the source of Q_3), and its drain is connected to ground.

Similar source-drain reversals occur for Q_4 except that here conditions are different for output short-circuit operation than during normal operation. Sensing circuitry monitors the voltages on the external capacitor's negative side and V_{OUT}, and compares them with ground. The substrate of Q_4 is then connected to the most negative of them. Figure 5 shows the substrate steering transistors for Q_3 and Q_4. The steering transistors ($Q_{S1\text{-}5}$) are relatively small n-channel devices, and share Q_3 and Q_4's substrates.

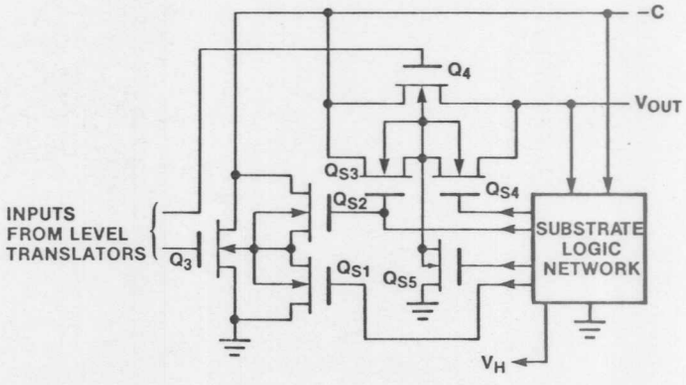


Figure 5. The substrate logic network

SCR Latch Up

A CMOS device is inherently a four-layer, or silicon-controlled-rectifier (SCR), structure. This structure can be turned on through the forward biasing of the inherent pn junctions, and unless external current-limiting circuitry is used, latchup and resultant failure can occur.

The n-channel transistor source acts as the cathode of the SCR, and the p+ source of the p-channel transistor acts as the anode. Either n- or p- channel drains can act as the SCR gate. With about 2 V or more across the anode and cathode, the SCR can have either a low-impedance (ON) or high-impedance (OFF) state. For the ON state to occur, three things must happen: the product of the transistors' current gains, or betas, must be at least unity, a current greater than the holding current must be present, and a trigger pulse must be applied to either gate of the SCR. Trigger signals may be caused by static discharge on the gates or by connecting either gate to the power supplies before connecting power-supply lines to other terminals of the SCR. Even extremly high rates of voltage change across any two or more SCR pn junctions can produce latchup.

Triggering a CMOS SCR causes it to present an extremely low impedance (1 to 100 ohms) across the power supply. Unless the power supply is current-limited, the device latches up and is often destroyed, usually by the vaporization of one of the bonding wires.

Although 7660 output-section switching transients are mainly capacitive, they inject currents into the substrate. At high input supply voltages, these transients can forward-bias junctions associated with the p- well or the Q_4 substrate. This in turn may trigger the inherent SCR in Q_4 and the adjacent on-chip circuitry. The result is to rapidly discharge the reservoir capacitor.

After the reservoir capacitor is almost totally discharged and the current in the SCR has fallen below the holding value, the device again operates correctly, until the output voltage (reservoir capacitance voltage) reaches the same critical value, and the latchup phenomenon starts again. Since this effect occurs only during the start of the charge cycle, and not during the pump cycle, isolating the reservoir capacitor with an external diode at the V_{OUT} terminal prevents capacitor discharge. This is recommended when using the device at higher voltage and temperatures. Otherwise the substrate logic network prevents SCR triggering, which is therefore not a problem for most operating conditions.

BASIC APPLICATION

The applications of the ICL7660 are remarkably varied, especially considering the rather narrow nature of the basic device function.

The basic circuit is shown in Figure 6, and the output characteristics for 5V inversion in Figure 7. For light loads, the output voltage follows the input very precisely, while for heavier loads, the output can be viewed as having perfect inversion, plus an output resistance of about 55Ω.

Thus at 18mA load, the output voltage drops about 1V below the input. Beyond around 40mA, the voltage drop becomes

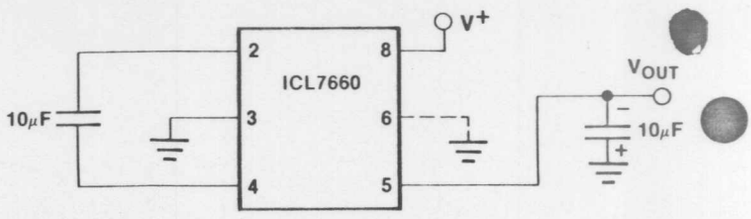


Figure 6. Simple Negative Converter

very non-linear, and the circuit self-limits, thereby protecting itself against excessive power dissipation. The output ripple is dependant primarily upon the output capacitor, since this must hold up the load during half the cycle time (or one oscillator period). In the steady-state case, this ripple is made up during the other half cycle time, and enough pump capacitance should be used to ensure that this is done monotonically. The recommended values ensure this for the internal oscillator frequency.

For operation at low voltages, the output impedance begins to rise rather rapidly, as a result of reduced turn-on voltage on the MOSFET switches (Fig. 8). This effect can be reduced by bypassing the internal regulator, tying LV to Ground, as shown in Figure 9. **This must not be done, however, if the incoming supply can exceed 6V under any circumstances, as the internal logic oscillator and divider stages will be damaged.** Note also the use of a series diode (Dx) at higher voltage and temperature, to protect the device against SCR action.

Figure 9 also shows an external oscillator capacitor. This can be used to reduce the oscillator frequency, giving a slight improvement in efficiency; see Figure 10.

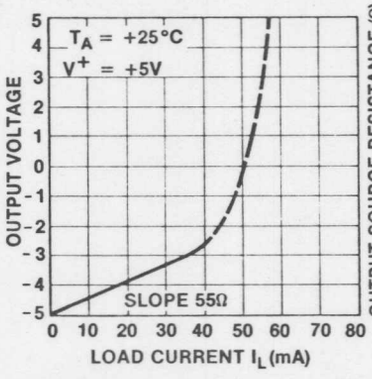


Figure 7. Output Characteristics

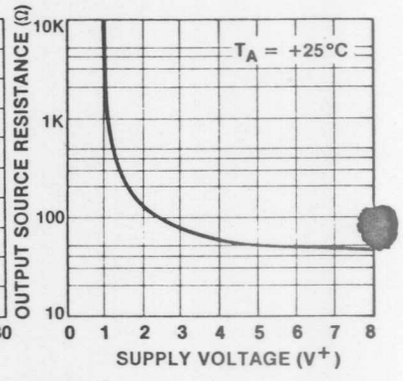


Figure 8. Output Resistance

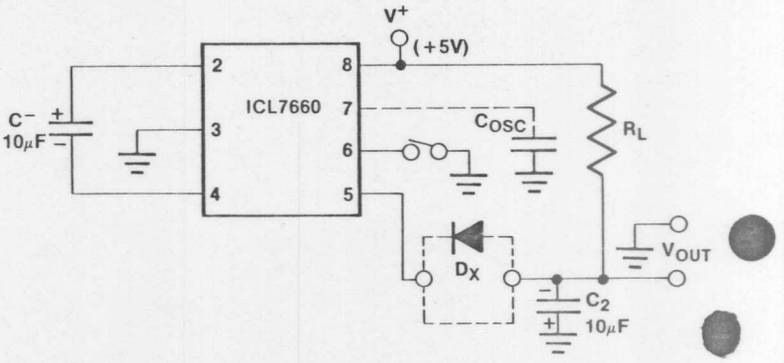


Figure 9. Variations of Basic Circuit

to EMI in a system. However the output ripple will be increased, and the output impedance also unless the pump and storage capacitors are correspondingly increased.

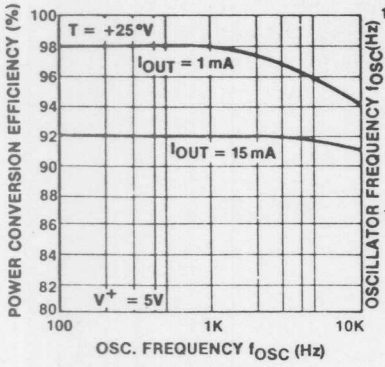


Figure 10. Efficiency Change with Oscillator Frequency

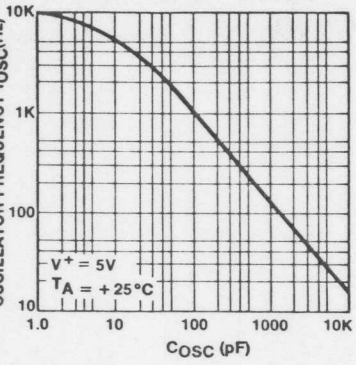


Figure 11. Frequency Variation with Oscillator Capacitance

Synchronization to an external clock can be readily achieved, as shown in Figure 12. A TTL device can be used with the addition of a pull-up resistor (10kΩ to V + is suitable), as can any input swinging rail-to-rail on the positive supply. The series resistor prevents problems with overdrive on the internal logic. Output transitions occur on the positive edge of the external input.

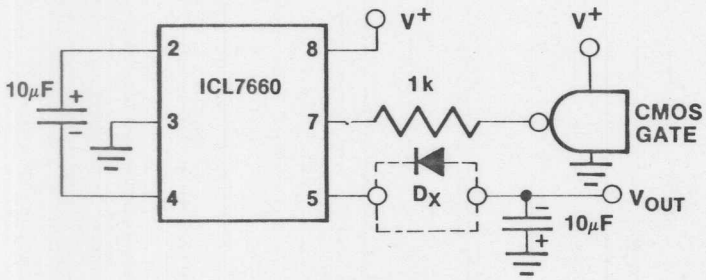


Figure 12. External Clocking

...IDER (Parallel Connections)

For applications where the voltage drop due to load current is excessive, several ICL7660s can be paralleled. Normally this cannot be done efficiently with power supply circuits, since each one has a different idea of where the "ideal" output voltage would be and they usually end up fighting each other. However, here they see equal input voltages, and the virtually perfect inversion assures that each one does have the same idea of where the output should be so load-sharing is assured. Each device must have a separate pump capacitor, since the oscillators cannot be synchronized except with an external drive, and even then the ÷2 will be in a random condition. The connections are shown in Figure 13. Naturally the output capacitor is common to each device. Running independently, the ripple content will include components at the difference frequency as well as the individual pumping frequencies. If this is undesirable, a single exclusive NOR gate can be used to put two ICL7660s into antiphase by comparing the outputs on pin 2, and clocking one to maintain near synchronization with the basic oscillator of the other, as shown in Figure 14.

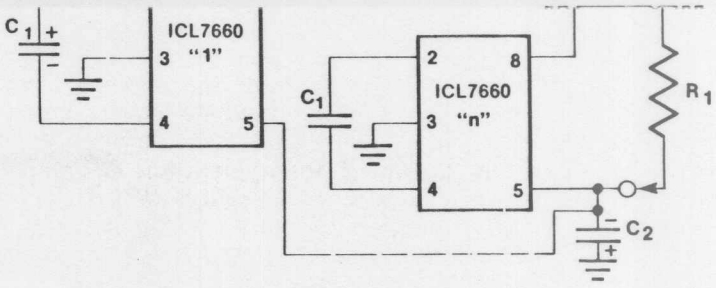


Figure 13. Paralleling Devices

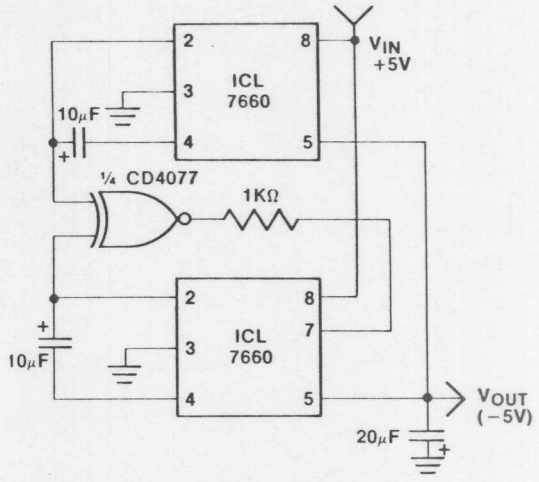


Figure 14. Synchronizing Two ICL7660s

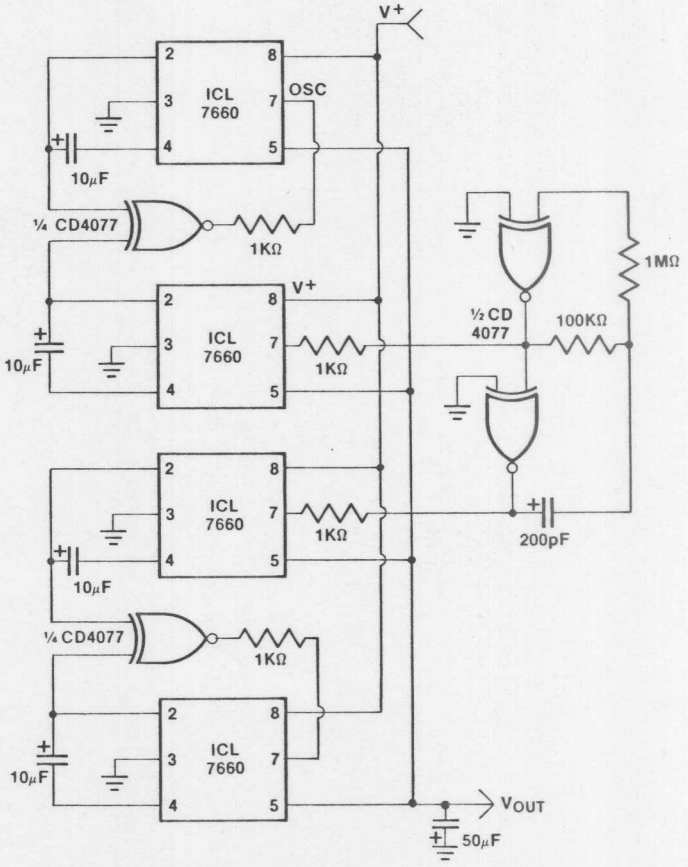


Figure 15. Synchronizing a Quad

The concept can be extended to drive four devices in four separate phases, using a single extra logic-gate package, as shown in Figure 15. The duty cycle of the oscillator is reasonably close to 50%, so driving two pairs, each in the configuration of Figure 14, from opposite phases of the oscillator gives four separately-timed pumps per cycle. This circuit will give about 75mA output before the voltage drops by 1V, or an output impedance of under 14Ω. The four-phase operation minimizes the ripple, while ensuring very even load sharing. For even more parallel synchronous device, a Johnson counter using Q and Q outputs should be considered.

DEEPER (Series Connection)

It is also possible to connect ICL7660s in series, cascading them to generate higher negative voltages. The basic connections are shown in Figure 16.

This technique can be extended to several multiplication levels. However, the basic limitations of this technique must be recognized. In line with the Laws of Thermodynamics, the input current required for each stage is twice the load current on that stage, plus the quiescent current required to operate that stage.

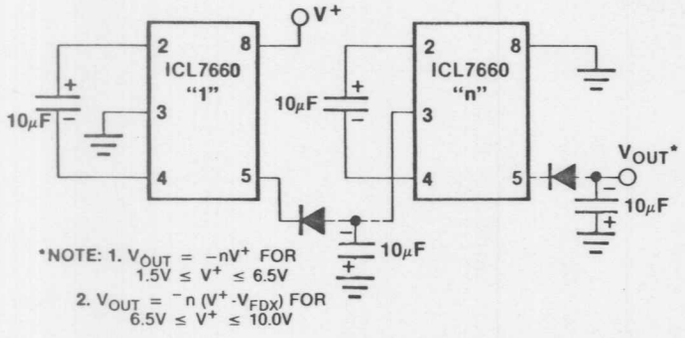


Figure 16. Cascading Devices for Increased Output Voltage

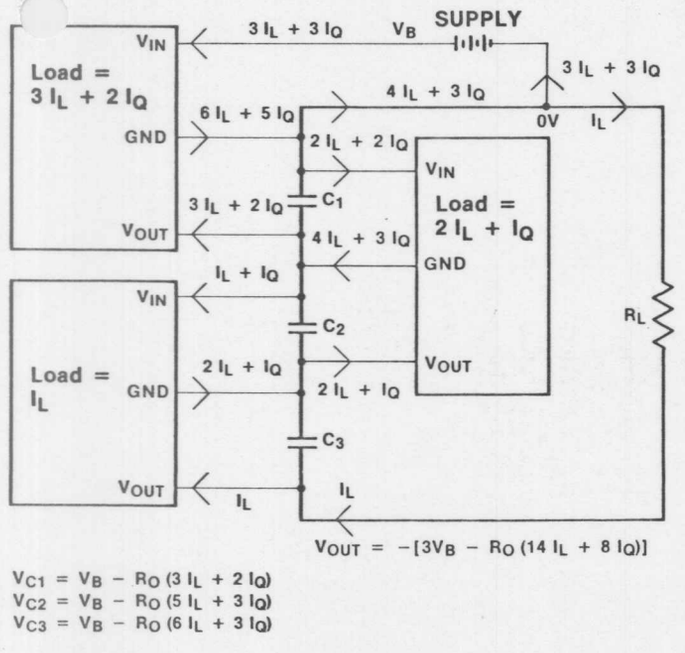


Figure 17. Current Flow for Cascaded Devices

Thus the load current is rapidly multiplied down the chain, as shown in Figure 17. Note also that the quiescent current increases the load current on each stage, though not as fast as the ultimate load itself.

Furthermore, the loss in voltage in early stages due to series resistance is multiplied through all subsequent stages. Thus the effective output impedance mounts rapidly with the number of stages. (See Table I) This effect can be reduced by paralleling devices in the lowest stages (see above.) If the weighting corresponds to the square of the position, the effective resistance to load current goes up only linearly with the number of stages, but the cost quickly becomes prohibitive. Nevertheless, for light loads and moderate multiplication, useful performance can be achieved.

TABLE 1

# stages	Resistance Multipliers	
n	R_O(L)	R_O(Q)
1	1	0
2	5	2
3	14	8
4	30	20
5	55	40
.	.	.
.	.	.
.	.	.

A variation of this circuit, another form of series circuit, is shown in Figure 18. This circuit can be used effectively to generate −15V from +5V in light load applications using only two devices. The output impedance corresponds roughly to n = 2 in Table 1, much better than if the previous circuit were used with n = 3. In general, geometric increases, as in Figure 18, are better until the voltage limit is reached, at which time arithmetic cascading as in Figure 16 must be utilized.

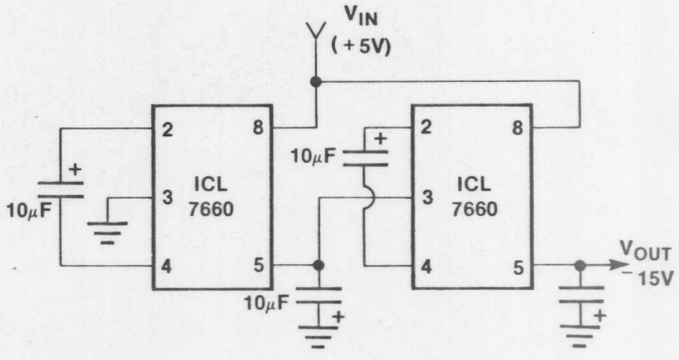


Figure 18. Getting −15V from −5V

UPSIDE DOWN (Positive Multiplication)

Up to this point, the ICL7660 has been used to multiply voltages in the negative direction. Clearly it would be possible to piggyback a standard diode pump onto a device, as in Figure 19, to generate a positive voltage. But the efficiency is not good, nor is the output impedance. However, the bidirectional nature of the MOSFET switches allows another more efficient circuit. The basic circuit can be run backwards, with the only problem being oscillator startup. The oscillator has no power supply until the circuit has been going enough to generate it, which it will not do until the oscillator is running, which won't happen until it

has a supply, which..... Fortunately, the exit from the this loop is easily arranged, as shown in Figure 20. Here, a small current is injected into the "LV" pin, enough to start the oscillator and drive the switches via the external diode and resistor. Once the circuit is operating, the diode becomes reverse biased and the resistor current is so small as to be almost irrelevant. Note that the quiescent current must be supplied through the pumping capacitor, adding to the driven load.

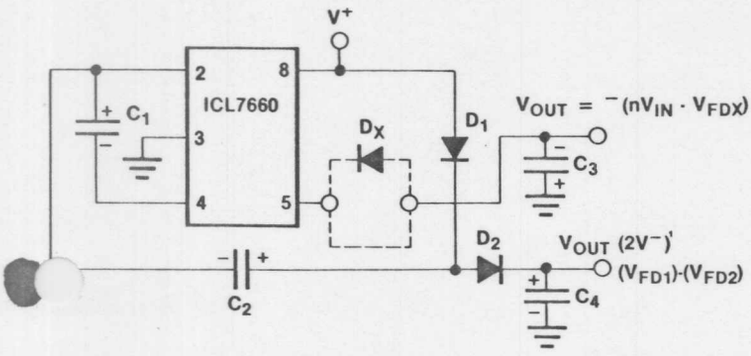


Figure 19. Combined Negative Converter and Positive Multiplier

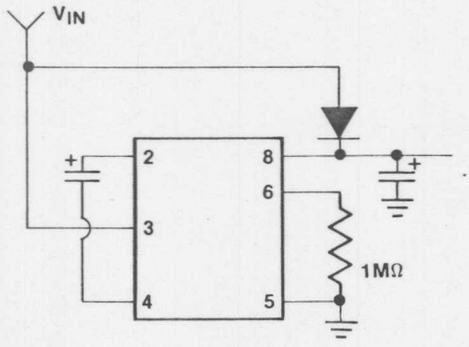


Figure 20. Resistor Start-up Circuit for Positive Multiplier

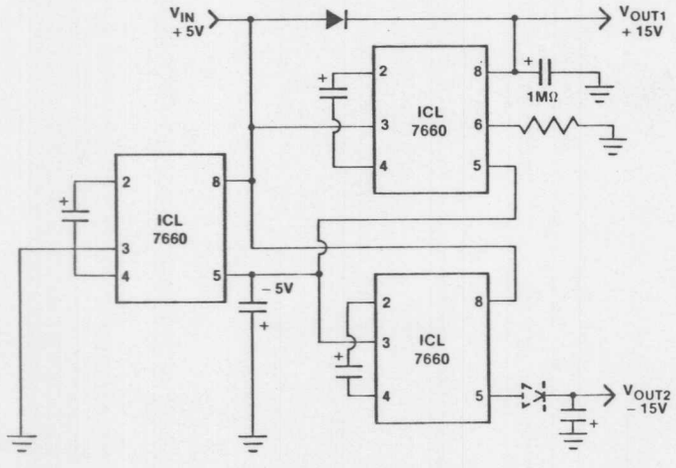


Figure 21. ±15V from +5V

This circuit can be stacked in parallel and in series in essentially the same way as before. For the parallel connection, generally only one device needs starting, since that one will pull up the others into operation. But for series connections, a separate start-up circuit will be needed for each level. The output impedances of these circuits are virtually identical to those of the corresponding negative multiplication arrangements.

Combinations of positive and negative multipliers can provide convenient functions such as those performed by the circuit in Figure 21, which generates ±15V from a +5V input. The operation is an extension of that shown in Figure 18, and the total output impedance, assuming equal loads on the ±15V supplies, is (per Table I) 11 times R_0 for load current, and 7 times for quiescent current.

DIVIDE and CONQUER

The same bidirectionality also allows the ICL7660 to be used to split a supply in half, as shown in Figure 22.

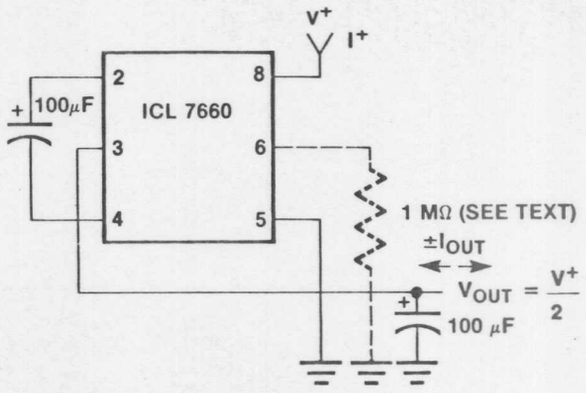


Figure 22. Efficient Supply Splitting

Here the "basic" output connection and the "basic" negative supply input are exchanged, and the output voltage thus becomes the midpoint. Once again, start-up can be a problem, and although careful capacitance and load balancing may frequently be adequate, a simple resistor to LV will always work. The circuit is useful for series-fed line systems, where a heavy local load at low voltage can be converted to a lighter current, at high voltage. Other useful applications are in driving low voltage (eg ±7.5V) circuits from ±15V supplies, or low voltage logic from 9V or 12V batteries. The output impedance is extremely low; all parts of the circuit cooperate in sharing the current, and so act in parallel.

For other division ratios, the series configurations of Figure 16 can be driven backwards, to generate V_{in}/n, or even $m/n(V_{in})$, for small values of m and n. Again, care must be taken to ensure start up for each device.

One interesting combination of several preceding circuits is shown in Figure 23, where a +15V supply is converted, via +7.5V and −7.5V, to −15V using three ICL7660s. The output impedance of this circuit is about 250Ω.

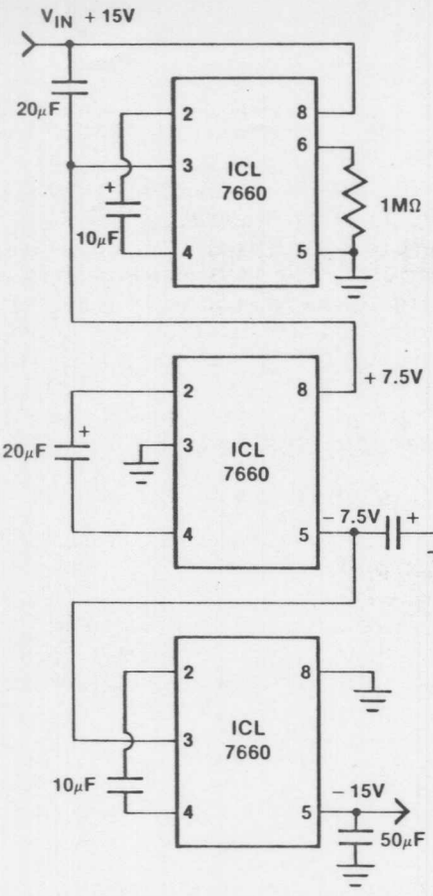


Figure 23. +15V to −15V in Three Easy Stages

For cases where the output impedance of an ICL7660 circuit is too high, obviously some form of output regulation can be used. However in most cases adequate regulation can be achieved at high efficiency by pre-regulating the input. A suitable circuit is shown in Figure 24, using the ICL7611 low power CMOS op amp. Because of the large source-current capability of this op amp, even on its lowest bias current setting, very efficient operation is possible. An ICL8069 band-gap device is used as the reference generator for the regulator. The output impedance can be reduced to 4Ω, while maintaining a current capability of well over 10mA. In designing circuits of this type, it is important to remember that there is a switching delay averaging one oscillator cycle between the output of the op amp and the actual output voltage. This can have substantial repercussions on the transient response if the time-constants in the circuit are not adequate. If multiple voltage converters are used, synchronization schemes such as those of Figures 14 and 15 are probably advisable.

MESSING ABOUT

The applications shown so far have corresponded to the use of the ICL7660 as a sort of equivalent of single turns on a power transformer, with paralleled turns to get more current, series turns for more voltage, etc. However, there are some other possibilities. By looking again at the block diagram (Figure 2), it is evident that the device could be used as a 50% duty cycle high power clock driver, using either the internal oscillator or an external signal, as in Figure 25. An antiphase clock can also be derived from the circuit, as shown, but the pull-up on this output, being an N-channel switch only, does not have as good a voltage swing. It is adequate for TTL level operation, but for CMOS clocking may require an external pull-up resistor or transistor.

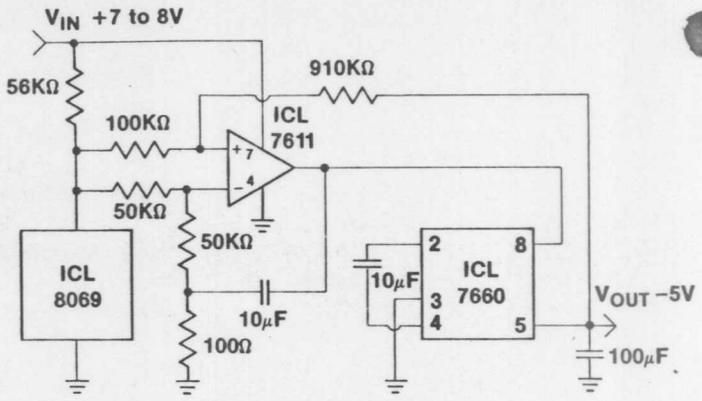


Figure 24. Regulated Output Inverter

Another interesting class of applications comes from the capability to synchronously detect the the output of an AC driven transducer, as shown in Figure 26. (This could be viewed as a signal transformer application.) Although the circuit shown utilizes a linear transformer type of transducer, any similar device may be used. The output voltage, which is correctly phased and of either polarity, may be fed into an A/D converter such as an ICL106/7 or ICL7109, for display or microprocessor interface as desired.

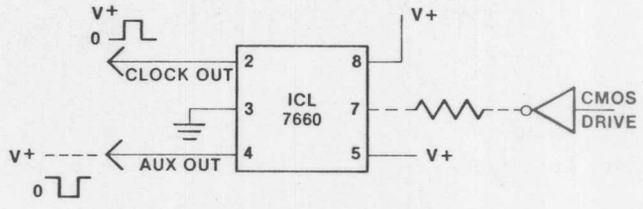


Figure 25. High power Clock Drive

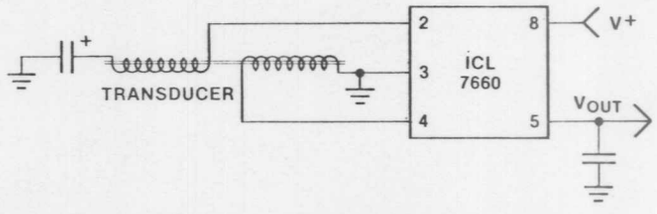


Figure 26. Transducer Driver and Detector

Some of this material was orginally presented at MIDCON '80 and SOUTHCON '81.

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